



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

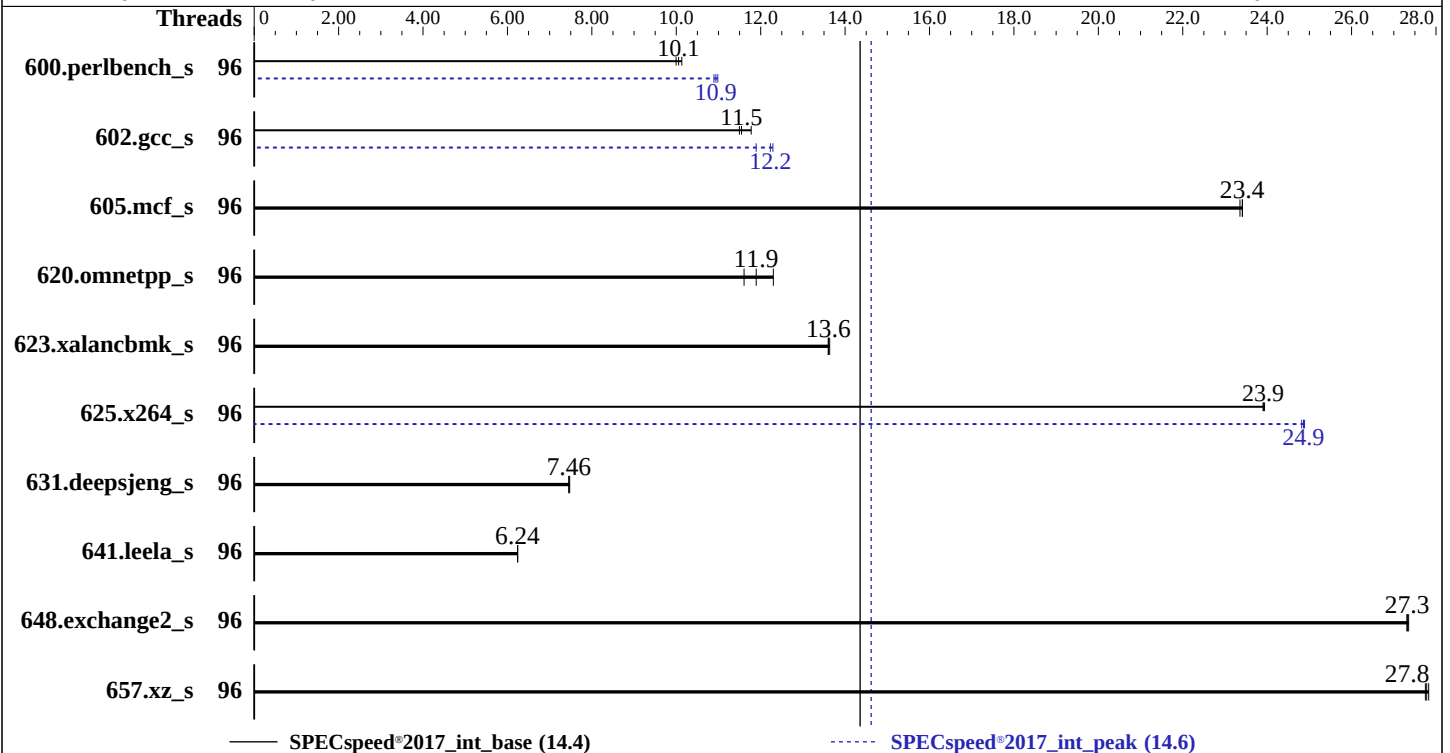
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024



Hardware

CPU Name: Intel Xeon 6520P
Max MHz: 4000
Nominal: 2400
Enabled: 48 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 64 KB I + 48 KB D on chip per core
L2: 2 MB I+D on chip per core
L3: 144 MB I+D on chip per chip
Other: None
Memory: 1 TB (16 x 64 GB 2Rx4 PC5-6400B-R)
Storage: 1 x 445 GB SATA SSD
Other: CPU Cooling: Air

Software

OS: SUSE Linux Enterprise Server 15 SP6
6.4.0-150600.21-default
Compiler: C/C++: Version 2024.1 of Intel oneAPI DPC++/C++ Compiler for Linux;
Fortran: Version 2024.1 of Intel Fortran Compiler for Linux;
Parallel: Yes
Firmware: Version 4.3.6a released Mar-2025
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	96	175	10.1	<u>177</u>	<u>10.1</u>	178	9.99	96	<u>162</u>	<u>10.9</u>	163	10.9	162	11.0
602.gcc_s	96	338	11.8	346	11.5	<u>345</u>	<u>11.5</u>	96	324	12.3	<u>326</u>	<u>12.2</u>	335	11.9
605.mcf_s	96	202	23.4	<u>202</u>	<u>23.4</u>	202	23.4	96	202	23.4	<u>202</u>	<u>23.4</u>	202	23.4
620.omnetpp_s	96	<u>137</u>	<u>11.9</u>	141	11.6	133	12.3	96	<u>137</u>	<u>11.9</u>	141	11.6	133	12.3
623.xalancbmk_s	96	104	13.6	<u>104</u>	<u>13.6</u>	104	13.6	96	104	13.6	<u>104</u>	<u>13.6</u>	104	13.6
625.x264_s	96	73.8	23.9	<u>73.8</u>	<u>23.9</u>	73.7	23.9	96	<u>71.0</u>	<u>24.9</u>	71.1	24.8	70.9	24.9
631.deepsjeng_s	96	192	7.47	<u>192</u>	<u>7.46</u>	192	7.45	96	192	7.47	<u>192</u>	<u>7.46</u>	192	7.45
641.leela_s	96	273	6.24	273	6.24	<u>273</u>	<u>6.24</u>	96	273	6.24	273	6.24	<u>273</u>	<u>6.24</u>
648.exchange2_s	96	107	27.4	<u>108</u>	<u>27.3</u>	108	27.3	96	107	27.4	<u>108</u>	<u>27.3</u>	108	27.3
657.xz_s	96	222	27.8	<u>223</u>	<u>27.8</u>	223	27.7	96	222	27.8	<u>223</u>	<u>27.8</u>	223	27.7

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,scatter"

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"

MALLOC_CONF = "retain:true"

OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM

memory using Redhat Enterprise Linux 8.0

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

sync; echo 3> /proc/sys/vm/drop_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS settings:

Sub NUMA clustering set to Enabled

Hardware prefetcher set to Enabled

Adjacent cache line prefetcher set to Enabled

XPT prefetch set to Auto

LLC prefetch set to Enabled

Enhanced CPU performance set to Auto

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6732 of 2022-11-07 fe91c89b7ed5c36ae2c92cc097bec197

running on c240m8-spec1 Mon May 12 13:12:13 2025

SUT (System Under Test) info as seen by some common utilities.

Table of contents

-
1. uname -a
 2. w
 3. Username
 4. ulimit -a
 5. sysinfo process ancestry
 6. /proc/cpuinfo
 7. lscpu
 8. numactl --hardware
 9. /proc/meminfo
 10. who -r
 11. Systemd service manager version: systemd 254 (254.10+suse.84.ge8d77af424)
 12. Services, from systemctl list-unit-files
 13. Linux kernel boot-time arguments, from /proc/cmdline
 14. cpupower frequency-info
 15. tuned-adm active
 16. sysctl
 17. /sys/kernel/mm/transparent_hugepage
 18. /sys/kernel/mm/transparent_hugepage/khugepaged
 19. OS release
 20. Disk information
 21. /sys/devices/virtual/dmi/id
 22. dmidecode
 23. BIOS
-

-
1. uname -a
Linux c240m8-spec1 6.4.0-150600.21-default #1 SMP PREEMPT_DYNAMIC Thu May 16 11:09:22 UTC 2024 (36c1e09)
x86_64 x86_64 x86_64 GNU/Linux
-

2. w
13:12:13 up 6 min, 3 users, load average: 0.00, 0.02, 0.00

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

USER	TTY	FROM	LOGIN@	IDLE	JCPU	PCPU	WHAT
root	tty1	-	13:07	5.00s	0.97s	0.00s	-bash
root	pts/0	10.29.148.129	13:10	29.00s	0.02s	0.02s	-bash

3. Username

From environment variable \$USER: root

4. ulimit -a

```
core file size          (blocks, -c) unlimited
data seg size           (kbytes, -d) unlimited
scheduling priority     (-e) 0
file size               (blocks, -f) unlimited
pending signals         (-i) 4125045
max locked memory       (kbytes, -l) 8192
max memory size         (kbytes, -m) unlimited
open files              (-n) 1024
pipe size                (512 bytes, -p) 8
POSIX message queues    (bytes, -q) 819200
real-time priority      (-r) 0
stack size              (kbytes, -s) unlimited
cpu time                (seconds, -t) unlimited
max user processes      (-u) 4125045
virtual memory          (kbytes, -v) unlimited
file locks              (-x) unlimited
```

5. sysinfo process ancestry

```
/usr/lib/systemd/systemd --switched-root --system --deserialize=42
login -- root
-bash
-bash
runcpu --nobuild -n 3 --action validate --define default-platform-flags --configfile
ic2024.1-lin-sapphirerapids-speed-20240308.cfg --define cores=96 --tune base --output_format all --define
intspeedaffinity --define drop_caches --nopower --runmode speed --tune base,peak --size refspeed intspeed
runcpu --nobuild --iterations 3 --action validate --define default-platform-flags --configfile
ic2024.1-lin-sapphirerapids-speed-20240308.cfg --define cores=96 --tune base --output_format all --define
intspeedaffinity --define drop_caches --nopower --runmode speed --tune base,peak --size refspeed --nopower
--runmode speed --tune base,peak --size refspeed intspeed --nopreenv --note-preenv --logfile
$SPEC/tmp/CPU2017.251/templogs/preenv.intspeed.251.0.log --lognum 251.0 --from_runcpu 2
specperl $SPEC/bin/sysinfo
$SPEC = /home/cpu2017
```

6. /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) 6520P
vendor_id      : GenuineIntel
cpu family     : 6
model          : 173
stepping       : 1
microcode      : 0x1000380
bugs           : spectre_v1 spectre_v2 spec_store_bypass swapgs bhi
cpu cores      : 24
siblings       : 48
2 physical ids (chips)
96 processors (hardware threads)
physical id 0: core ids 0-23
physical id 1: core ids 0-23
physical id 0: apicids 0-47
```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

physical id 1: apicids 128-175

Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for virtualized systems. Use the above data carefully.

7. lscpu

From lscpu from util-linux 2.39.3:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Address sizes:         46 bits physical, 57 bits virtual
Byte Order:            Little Endian
CPU(s):                96
On-line CPU(s) list:   0-95
Vendor ID:              GenuineIntel
BIOS Vendor ID:        Intel(R) Corporation
Model name:             Intel(R) Xeon(R) 6520P
BIOS Model name:       Intel(R) Xeon(R) 6520P   CPU @ 2.4GHz
BIOS CPU family:       179
CPU family:             6
Model:                 173
Thread(s) per core:    2
Core(s) per socket:    24
Socket(s):              2
Stepping:               1
CPU(s) scaling MHz:    31%
CPU max MHz:           4000.0000
CPU min MHz:           800.0000
BogoMIPS:               4800.00
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat
                        pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
                        pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good
                        nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni
                        pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
                        xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                        tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm
                        3dnowprefetch cpuid_fault epb cat_l3 cat_l2 cdp_l3 intel_ppin cdp_l2
                        ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow flexpriority ept
                        vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
                        rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt
                        clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec
                        xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
                        split_lock_detect user_shstk avx_vnni avx512_bf16 wbnoinvd dtherm ida
                        arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req hfi vnni
                        avx512vbmi umip pku ospke waitpkg avx512_vbmi2 gfni vaes vpclmulqdq
                        avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid
                        bus_lock_detect cldemote movdiri movdir64b enqcmd fsrm md_clear
                        serialize tsxldtrk pconfig arch_lbr ibt amx_bf16 avx512_fp16 amx_tile
                        amx_int8 flush_l1d arch_capabilities
Virtualization:         VT-x
L1d cache:              2.3 MiB (48 instances)
L1i cache:              3 MiB (48 instances)
L2 cache:               96 MiB (48 instances)
L3 cache:               288 MiB (2 instances)
NUMA node(s):           2
NUMA node0 CPU(s):      0-23,48-71
NUMA node1 CPU(s):      24-47,72-95
Vulnerability Gather data sampling: Not affected
Vulnerability Itlb multihit:      Not affected
Vulnerability L1tf:           Not affected
```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

Vulnerability Mds:	Not affected
Vulnerability Meltdown:	Not affected
Vulnerability Mmio stale data:	Not affected
Vulnerability Reg file data sampling:	Not affected
Vulnerability Retbleed:	Not affected
Vulnerability Spec rstack overflow:	Not affected
Vulnerability Spec store bypass:	Mitigation; Speculative Store Bypass disabled via prctl
Vulnerability Spectre v1:	Mitigation; usercopy/swaps barriers and __user pointer sanitization
Vulnerability Spectre v2:	Mitigation; Enhanced / Automatic IBRS; IBPB conditional; RSB filling; PBRSE-eIBRS Not affected; BHI BHI_DIS_S
Vulnerability Srbds:	Not affected
Vulnerability Tsx async abort:	Not affected

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	48K	2.3M	12	Data	1	64	1	64
L1i	64K	3M	16	Instruction	1	64	1	64
L2	2M	96M	16	Unified	2	2048	1	64
L3	144M	288M	16	Unified	3	147456	1	64

8. numactl --hardware

NOTE: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0-23,48-71
node 0 size: 515264 MB
node 0 free: 513962 MB
node 1 cpus: 24-47,72-95
node 1 size: 516023 MB
node 1 free: 515008 MB
node distances:
node  0  1
 0:  10  21
 1:  21  10
```

9. /proc/meminfo

MemTotal: 1056038748 kB

10. who -r

run-level 3 May 12 13:05

11. Systemd service manager version: systemd 254 (254.10+suse.84.ge8d77af424)

Default Target	Status
multi-user	running

12. Services, from systemctl list-unit-files

STATE	UNIT FILES
enabled	YaST2-Firstboot YaST2-Second-Stage apparmor auditd cron display-manager getty@ irqbalance issue-generator kbdsettings klog lvm2-monitor nsd postfix purge-kernels rollback rsyslog sep5 smartd sshd systemd-pstore wicked wickedd-auto4 wickedd-dhcp4 wickedd-dhcp6 wickedd-nanny
enabled-runtime	systemd-remount-fs
disabled	autofs autoyast-initscripts blk-availability boot-sysctl ca-certificates chrony-wait chronyd console-getty cups cups-browsed debug-shell ebttables exchange-bmc-os-info firewallld fsidd gpm grub2-once haveged ipmi ipmievd issue-add-ssh-keys kexec-load lunmask man-db-create multipathd nfs nfs-blkmap rpcbind rpmconfigcheck rsyncd serial-getty@

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

indirect
smartrd_generate_opts snmpd snmptrapd systemd-boot-check-no-failures systemd-confext
systemd-network-generator systemd-sysexit systemd-time-wait-sync systemd-timesyncd tuned
udisks2 vncserver@
systemd-userdbd wickedd

13. Linux kernel boot-time arguments, from /proc/cmdline
BOOT_IMAGE=/boot/vmlinuz-6.4.0-150600.21-default
root=UUID=52f44b73-418f-485e-abb1-6b40f358d6a0
splash=silent
mitigations=auto
quiet
security=apparmor

14. cpupower frequency-info
analyzing CPU 79:
current policy: frequency should be within 800 MHz and 4.00 GHz.
The governor "performance" may decide which speed to use
within this range.
boost state support:
Supported: yes
Active: yes

15. tuned-adm active
No current active profile.

16. sysctl
kernel.numa_balancing 1
kernel.randomize_va_space 2
vm.compaction_proactiveness 20
vm.dirty_background_bytes 0
vm.dirty_background_ratio 10
vm.dirty_bytes 0
vm.dirty_expire_centisecs 3000
vm.dirty_ratio 20
vm.dirty_writeback_centisecs 500
vm.dirtytime_expire_seconds 43200
vm.extfrag_threshold 500
vm.min_unmapped_ratio 1
vm.nr_hugepages 0
vm.nr_hugepages_mempolicy 0
vm.nr_overcommit_hugepages 0
vm.swappiness 60
vm.watermark_boost_factor 15000
vm.watermark_scale_factor 10
vm.zone_reclaim_mode 0

17. /sys/kernel/mm/transparent_hugepage
defrag always defer defer+madvice [madvice] never
enabled [always] madvice never
hpage_pmd_size 2097152
shmem_enabled always within_size advise [never] deny force

18. /sys/kernel/mm/transparent_hugepage/khugepaged
alloc_sleep_millisecs 60000

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

defrag 1
max_ptes_none 511
max_ptes_shared 256
max_ptes_swap 64
pages_to_scan 4096
scan_sleep_millisecs 10000

19. OS release
From /etc/*-release /etc/*-version
os-release SUSE Linux Enterprise Server 15 SP6

20. Disk information
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdc2 xfs 445G 54G 391G 13% /

21. /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M8SX
Serial: WZP28449MSW

22. dmidecode
Additional information from dmidecode 3.4 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
16x 0xCE00 M321R8GA0PB2-CCPEC 64 GB 2 rank 6400

23. BIOS
(This section combines info from /sys/devices and dmidecode.)
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M8.4.3.6a.0.0319250402
BIOS Date: 03/19/2025
BIOS Revision: 5.35

Compiler Version Notes

C | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak)
| 657.xz_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak)
| 641.leela_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Compiler Version Notes (Continued)

=====

Fortran | 648.exchange2_s(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -fiopenmp
-DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:

-w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Base Optimization Flags (Continued)

Fortran benchmarks:

-w -m64 -wl, -z, muldefs -xsapphirerapids -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -w -m64 -std=c11 -wl, -z, muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast(pass 1) -xCORE-AVX512 -O3 -ffast-math
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-fiopenmp -DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -w -m64 -std=c11 -wl, -z, muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast(pass 1) -xCORE-AVX512 -O3 -ffast-math
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6520P 2.40 GHz processor)

SPECspeed®2017_int_base = 14.4

SPECspeed®2017_int_peak = 14.6

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Peak Optimization Flags (Continued)

602.gcc_s (continued):

-fiopenmp -DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -w -std=c11 -m64 -WL,-z,muldefs -xsapphirerapids -O3
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fiopenmp -DSPEC_OPENMP
-fno-alias -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.2025-06-17.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-GNR-revD.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.2025-06-17.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-GNR-revD.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.9 on 2025-05-12 16:12:12-0400.

Report generated on 2025-06-17 18:11:41 by CPU2017 PDF formatter v6716.

Originally published on 2025-06-17.