



# SPEC® CPU2017 Floating Point Rate Result

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## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5115  
2.40 GHz)

**SPECrate2017\_fp\_base = 121**

**SPECrate2017\_fp\_peak = Not Run**

**CPU2017 License:** 9019

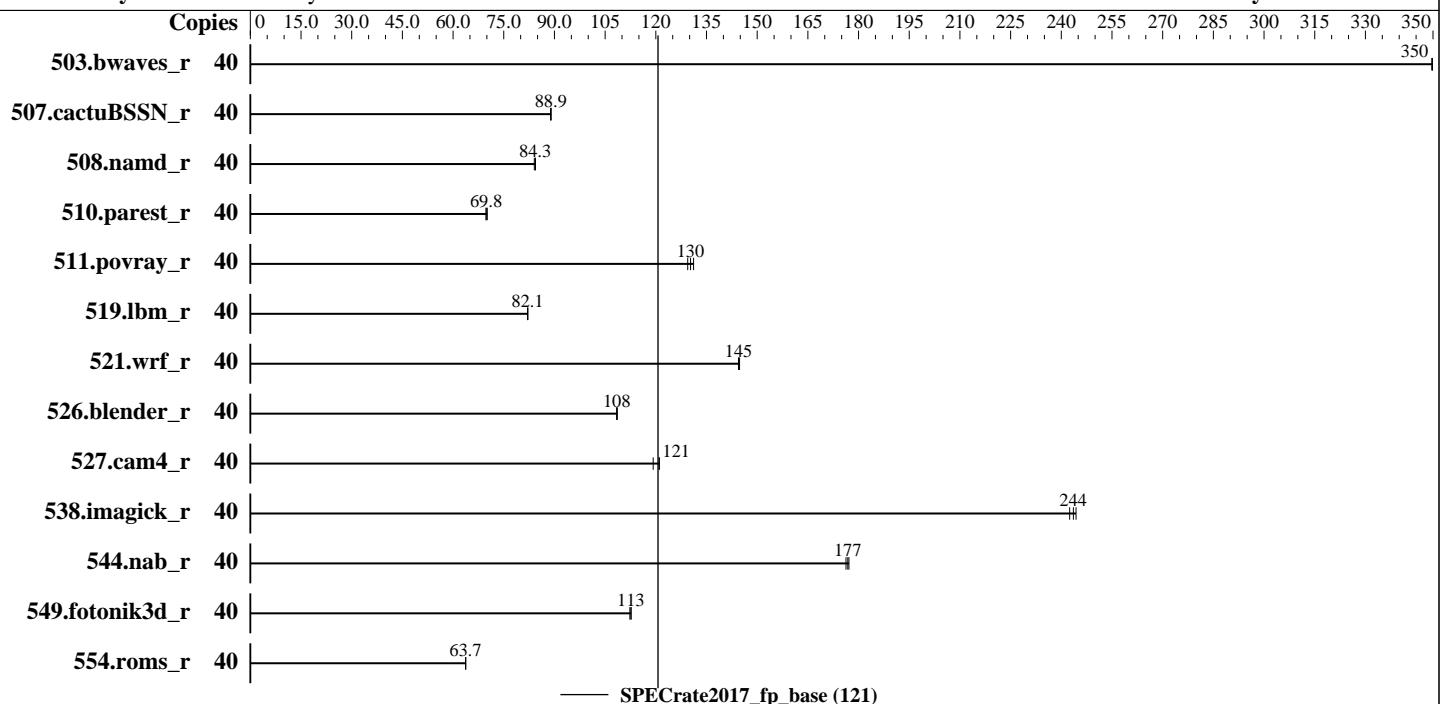
**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Nov-2018



### Hardware

CPU Name: Intel Xeon Gold 5115  
Max MHz.: 3200  
Nominal: 2400  
Enabled: 20 cores, 2 chips, 2 threads/core  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 13.75 MB I+D on chip per chip  
Other: None  
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R,  
running at 2400)  
Storage: 1 x 240 GB M.2 SATA SSD  
Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP3 (x86\_64)  
4.4.120-94.17-default  
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++  
Compiler for Linux;  
Fortran: Version 19.0.1.144 of Intel Fortran  
Compiler for Linux  
Parallel: No  
Firmware: Version 4.0.1 released Oct-2018  
File System: xfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: Not Applicable  
Other: None



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	40	<b>1147</b>	<b>350</b>	1147	350	1147	350							
507.cactuBSSN_r	40	570	88.9	569	89.0	<b>570</b>	<b>88.9</b>							
508.namd_r	40	<b>451</b>	<b>84.3</b>	450	84.4	452	84.0							
510.parest_r	40	1492	70.1	<b>1499</b>	<b>69.8</b>	1500	69.8							
511.povray_r	40	722	129	<b>717</b>	<b>130</b>	712	131							
519.lbm_r	40	513	82.1	<b>514</b>	<b>82.1</b>	514	82.1							
521.wrf_r	40	620	144	619	145	<b>620</b>	<b>145</b>							
526.blender_r	40	562	108	<b>562</b>	<b>108</b>	561	109							
527.cam4_r	40	578	121	<b>578</b>	<b>121</b>	587	119							
538.imagick_r	40	410	242	<b>408</b>	<b>244</b>	407	244							
544.nab_r	40	380	177	382	176	<b>381</b>	<b>177</b>							
549.fotonik3d_r	40	<b>1384</b>	<b>113</b>	1388	112	1383	113							
554.roms_r	40	997	63.7	<b>997</b>	<b>63.7</b>	998	63.7							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

sync; echo 3> /proc/sys/vm/drop\_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

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## General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-4dlf Thu Jan 24 10:55:19 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz

2 "physical id"s (chips)

40 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 10

siblings : 20

physical 0: cores 0 1 2 3 4 8 9 10 11 12

physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 40

On-line CPU(s) list: 0-39

Thread(s) per core: 2

Core(s) per socket: 10

Socket(s): 2

NUMA node(s): 2

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

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## Platform Notes (Continued)

Model name: Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz  
Stepping: 4  
CPU MHz: 1114.580  
CPU max MHz: 3200.0000  
CPU min MHz: 1000.0000  
BogoMIPS: 4788.75  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 14080K  
NUMA node0 CPU(s): 0-9,20-29  
NUMA node1 CPU(s): 10-19,30-39  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant\_tsc art arch\_perfmon pebs bts rep\_good nopl xtopology nonstop\_tsc aperfmpfperf eagerfpu pni pclmulqdq dtes64 monitor ds\_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4\_1 sse4\_2 x2apic movbe popcnt tsc\_deadline\_timer aes xsave avx f16c rdrand lahf\_lm abm 3dnowprefetch ida arat epb invpcid\_single pln pts dtherm hwp hwp\_act\_window hwp\_epp hwp\_pkg\_req intel\_pt rsb\_ctxsw spec\_ctrl stibp retpoline kaiser tpr\_shadow vnmi flexpriority ept vpid fsgsbase tsc\_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm\_llc cqm\_occup\_llc pkruospke

/proc/cpuinfo cache data  
cache size : 14080 KB

From numactl --hardware    WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29  
node 0 size: 385631 MB  
node 0 free: 385161 MB  
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39  
node 1 size: 387060 MB  
node 1 free: 386543 MB  
node distances:  
node 0 1  
0: 10 21  
1: 21 10

From /proc/meminfo  
MemTotal: 791236488 kB  
HugePages\_Total: 0  
Hugepagesize: 2048 kB

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## Platform Notes (Continued)

```
From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 3
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
os-release:
    NAME="SLES"
    VERSION="12-SP3"
    VERSION_ID="12.3"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP3"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp3"

uname -a:
Linux linux-4dlf 4.4.120-94.17-default #1 SMP Wed Mar 14 17:23:00 UTC 2018 (cf3a7bb)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2017-5754 (Meltdown): Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB
```

run-level 3 Jan 24 10:52

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdb2        xfs   220G   31G  189G  15%  /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.1.139.1003182107 10/03/2018

Memory:

```
7x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400
17x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400
```

(End of data from sysinfo program)



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## Compiler Version Notes

=====

CC 519.lbm\_r(base) 538.imagick\_r(base) 544.nab\_r(base)

=====

icc (ICC) 19.0.1.144 20181018

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=====

CXXC 508.namd\_r(base) 510.parest\_r(base)

=====

icpc (ICC) 19.0.1.144 20181018

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=====

CC 511.povray\_r(base) 526.blender\_r(base)

=====

icpc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

icc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====

FC 507.cactubSSN\_r(base)

=====

icpc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

icc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

ifort (IFORT) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====

FC 503.bwaves\_r(base) 549.fotonik3d\_r(base) 554.roms\_r(base)

=====

ifort (IFORT) 19.0.1.144 20181018

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=====

CC 521.wrf\_r(base) 527.cam4\_r(base)

=====

ifort (IFORT) 19.0.1.144 20181018

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## Compiler Version Notes (Continued)

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## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

## Base Portability Flags

503.bwaves\_r: -DSPEC\_LP64  
507.cactuBSSN\_r: -DSPEC\_LP64  
508.namd\_r: -DSPEC\_LP64  
510.parest\_r: -DSPEC\_LP64  
511.povray\_r: -DSPEC\_LP64  
519.lbm\_r: -DSPEC\_LP64  
521.wrf\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian  
526.blender\_r: -DSPEC\_LP64 -DSPEC\_LINUX -funsigned-char  
527.cam4\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG  
538.imagick\_r: -DSPEC\_LP64  
544.nab\_r: -DSPEC\_LP64  
549.fotonik3d\_r: -DSPEC\_LP64  
554.roms\_r: -DSPEC\_LP64



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## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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